PTO/SB/81 (04-05)
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Application Number	nrmation unless it displays a valid OMB control number. 10/722,686
Filing Date	November 24, 2003
First Named Inventor	Benware, Robert
Title	Self-Timed Scan Circuit for ASIC
Art Unit	2819
Examiner Name	Le, Don P.
Attorney Docket Number	03-1122

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Applicant/Inventor.								
Assignee of record of the entire interest. See 37 CFR 3.71.								
Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)								
SIGNATURE of Applicant or Assignee of Record								
Signature	N PA I				Date	9/20/05		
Name	Sandeep Jaggi / ()				Telephone	(408) 954-4923		
Title and Company Chief IP Counsel, Assistant Corporate Secretary, LSI Logic Corporation								
NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.								
*Total of1 forms are submitted.								

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

PTO/SB/96 (09-04) Approved for use through 07/31/2006. OMB 0651-0031

Telephone Number

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Applicant/Patent Owner: LSI Logic Corporation Application No./Patent No.: 10/722,686 Filed/Issue Date: November 24, 2003 Entitled: Self-Timed Scan Circuit for ASIC Fault Testing LSI Logic Corporation Corporation (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.) (Name of Assignee) states that it is: 1. 📊 the assignee of the entire right, title, and interest; or 2. an assignee of less than the entire right, title and interest. The extent (by percentage) of its ownership interest is____ in the patent application/patent identified above by virtue of either: An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 014761 , Frame 0725 , or for which a copy thereof is attached. A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as shown below: The document was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached. To: The document was recorded in the United States Patent and Trademark Office at _____, Frame ____ ____, or for which a copy thereof is attached. Reel __ To: The document was recorded in the United States Patent and Trademark Office at _____, Frame _____, or for which a copy thereof is attached. Additional documents in the chain of title are listed on a supplemental sheet.

STATEMENT UNDER 37 CFR 3.73(b)

Copies of assignments or other documents in the chain of title are attached.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, if the assignment is to be recorded in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

Signature Sandeep Jaggi (408) 954-4923

Printed or Typed Name

Chief IP Counsel, Assistant Corporate Secretary Title

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